EXPLICIT WAVE DIGITAL MODEL OF THE FULLTONE OCD PEDAL BASED ON CANONICAL PIECEWISE-LINEAR FUNCTIONS

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ABSTRACT

Virtual Analog (VA) modeling aims at digitally emulating analog audio equipment while preserving its characteristic nonlinear behavior and musical expressiveness. In the context of guitar effects, overdrive pedals represent a cornerstone of many signal chains, as they strongly contribute to the perceived dynamics, articulation, and timbral identity of the instrument. Among these, the Fulltone OCD overdrive is considered a standard in both studio and live environments, being widely adopted across rock and metal genres. In this article, we present an explicit Wave Digital (WD) model of the Fulltone OCD (v2) pedal. By exploiting the circuit topology, the MOSFETs and the germanium diode composing the asymmetric clipping stage are grouped into a single equivalent nonlinear element, enabling an explicit WD realization that avoids costly iterative solvers. The resulting nonlinear characteristic is approximated by means of a Canonical Piecewise-Linear (CPWL) function, yielding a compact and efficient explicit model suitable for real-time implementation. The proposed model is validated against reference simulations and implemented both in MATLAB and as a real-time audio plug-in using the JUCE framework.

1. INTRODUCTION

The advent of digital audio effects has profoundly transformed music production, performance, and sound design [1]. Nevertheless, a large community of musicians and producers continues to value the characteristics of analog audio equipment, especially when it comes to select electric guitar pedals, where nonlinearities play a crucial musical role. As a consequence, Virtual Analog (VA) modeling has emerged as a prominent research field, aiming at reproducing the behavior and sound of analog devices in the digital domain while retaining real-time capability and expressive control [1].

Over the years, two main paradigms have been adopted for VA modeling. On the one hand, *white-box* approaches rely on explicit knowledge of the circuit topology and component physics, typically formulating and solving systems of nonlinear differential or algebraic equations using state-space techniques [2, 3], Port-Hamiltonian methods [4], or Wave Digital Filters (WDFs) [5]. On the other hand, *black-box* approaches aim at reproducing the input–output behavior of a device by means of system identification techniques, such as Volterra series [6], Wiener–Hammerstein models [7], or, more recently, machine learning-based methods [8, 9]. Hybrid approaches, instead, combine these strategies by embedding neural models into white-box structures [10, 11, 12, 13, 14, 15]. Within this landscape, nonlinear distortion and overdrive effects have received significant attention due to their widespread use and their strong impact on musical expressiveness [16, 7, 17]. Distortion and overdrive pedals are not merely signal processors, but musical instruments in their own right, shaping articulation, sustain, and dynamics [18]. In particular, overdrive effects play a crucial role in rock and metal music, where they contribute to playability, perceived virtuosity, and tonal identity [19]. Empirical and musicological studies have shown how distortion devices affect guitar performance practices and sound aesthetics, often serving as reference elements in controlled experiments and production workflows. Notably, the Fulltone OCD overdrive pedal has been repeatedly employed as a representative and musically meaningful overdrive device in experimental and analytical studies on guitar sound and performance practice [18, 19], further underlining its status as an industry standard.

From a circuital perspective, the Fulltone OCD stands out from many classic overdrive pedals due to its MOSFET-based clipping stage, which introduces asymmetrical saturation and a highly dynamic response reminiscent of tube amplifier breakup [19]. While this design choice is largely responsible for the pedal musical success, it also poses nontrivial challenges for digital emulation. The voltage-dependent resistance and nonlinear current–voltage characteristics of the MOSFETs lead to implicit relations that are demanding to solve efficiently in real time.

WDFs, originally introduced by Fettweis for the discretization of passive electrical networks [5], have proven to be a powerful framework for white-box VA modeling [17, 20, 21]. Their modular structure and clear separation between topology and element description make them particularly suitable for modeling nonlinear audio circuits [20]. However, classical WDF formulations typically allow for only a limited number of nonlinear ports without resorting to iterative solvers [22], which may compromise real-time performance.

In this work, we address these challenges by proposing an explicit Wave Digital (WD) model of the Fulltone OCD (v2) pedal based on Canonical Piecewise-Linear (CPWL) functions [23, 24]. Building upon recent advances in CPWL modeling in the WD domain, we approximate the nonlinear characteristics of the MOSFET-based clipping stage with a set of affine segments that admit closed-form wave mappings. This allows us to derive an explicit scattering formulation of the entire circuit [22], significantly reducing computational complexity while preserving physical interpretability and accuracy. Compared to iterative WD approaches [25, 20], the proposed model avoids runtime nonlinear solvers and is therefore well-suited for real-time audio applications. The proposed model is validated through comparisons with a reference simulation and is implemented both in MATLAB and in a JUCE-based audio plug-in, demonstrating its practical applicability in production environments.

The remainder of the paper is organized as follows. Section 2 reviews the theoretical background on WDFs and CPWL modeling. Section 3 deals with the modeling of diode-connected MOSFETs. Section 4 presents the WD iterative and explicit algorithms taken into account in this work. Finally, Section 5 discusses the WD implementation of the Fulltone OCD pedal, while Section 6 draws conclusions.

2. BACKGROUND ON WDFS

Let us recall fundamental WDF theory that will be employed in the development of the proposed model of the Fulltone OCD pedal. The WDF approach is based on a port-wise description of the reference circuit [5, 26]. At each port, the port voltage v and port current i, referred to as Kirchhoff variables, are transformed into an incident wave a and a reflected wave b through a suitable wave definition. Although several wave formulations have been introduced in the literature [5, 27, 28], this work adopts voltage waves, which remain the most commonly used representation. The corresponding linear mapping between Kirchhoff and wave variables is given by [5]

$$a = v + Zi\,, \qquad b = v - Zi\,, \tag{1}$$

where Z is a free parameter known as the *port resistance*. This quantity plays a pivotal role in the Wave Digital (WD) formulation, as it provides a key degree of freedom in the model design [5].

In the WDF framework, circuit elements and circuit topology are described separately by means of input-output blocks governed by scattering relations. When WD blocks are interconnected, instantaneous dependencies between incident and reflected waves may arise, resulting in delay-free loops (DFLs) [5]. Such implicit relations can be avoided by properly choosing the port resistances. In this case, the element or the junction port at which the DFL is eliminated is said to be *adapted*. Finally, it is worth emphasizing that port adaptation is generally possible only for linear elements; nonlinear components, therefore, require alternative modeling strategies [20].

2.1. Modeling Connection Networks

Topological junctions, also referred to as connection networks, are modeled as N-port WD blocks. Their behavior is described by a scattering relation of the form $\mathbf{a} = \mathbf{S}\mathbf{b}$ [5], where $\mathbf{S}$ is the scattering matrix, $\mathbf{a} = [a_1, \ldots, a_N]^{\mathrm{T}}$ is the vector of waves incident to the elements and reflected by the junction, and $\mathbf{b} = [b_1, \ldots, b_N]^{\mathrm{T}}$ collects the waves reflected by the elements and incident to the junction. Let us consider the case in which the topological junction is connected only to 1-port elements. The scattering matrix $\mathbf{S}$ can be derived by means of standard loop or cut-set analyses in the Kirchhoff domain, yielding one of the following equivalent expressions [29, 28]

$$\mathbf{S} = 2\mathbf{Q}^{\mathrm{T}}(\mathbf{Q}\mathbf{Z}^{-1}\mathbf{Q}^{\mathrm{T}})^{-1}\mathbf{Q}\mathbf{Z}^{-1} - \mathbf{I}\,, \tag{2}$$

$$\mathbf{S} = \mathbf{I} - 2\mathbf{Z}\mathbf{B}^{\mathrm{T}}(\mathbf{B}\mathbf{Z}\mathbf{B}^{\mathrm{T}})^{-1}\mathbf{B}\,, \tag{3}$$

where $\mathbf{I}$ denotes the $N \times N$ identity matrix, $\mathbf{Q}$ and $\mathbf{B}$ are the fundamental cut-set and loop matrices, respectively, and $\mathbf{Z}$ is a diagonal matrix containing the port resistances $[Z_1, \ldots, Z_N]$.

If operational amplifiers (opamps) are present in the circuit schematic, they can be replaced by their *nullor*-based models, which can be incorporated into the connection networks [30]. This substitution is valid under the assumption of ideal opamp behavior. From the resulting network representation, the so-called V-net and I-net can be derived [30], allowing the scattering matrix of the overall topology to be computed as [30]

$$\mathbf{S} = 2\mathbf{Q}_{\mathrm{V}}{}^{\mathrm{T}}(\mathbf{Q}_{\mathrm{I}}\mathbf{Z}^{-1}\mathbf{Q}_{\mathrm{V}}{}^{\mathrm{T}})^{-1}\mathbf{Q}_{\mathrm{I}}\mathbf{Z}^{-1} - \mathbf{I}\,, \tag{4}$$

$$\mathbf{S} = \mathbf{I} - 2\mathbf{Z}\mathbf{B}_{\mathrm{I}}{}^{\mathrm{T}}(\mathbf{B}_{\mathrm{V}}\mathbf{Z}\mathbf{B}_{\mathrm{I}}{}^{\mathrm{T}})^{-1}\mathbf{B}_{\mathrm{V}}\,, \tag{5}$$

where $\mathbf{Q}_{\mathrm{V}}$ and $\mathbf{Q}_{\mathrm{I}}$ are the fundamental cut-set matrices of the V-net and I-net, respectively, and $\mathbf{B}_{\mathrm{V}}$ and $\mathbf{B}_{\mathrm{I}}$ denote the corresponding fundamental loop matrices.

2.2. Modeling Linear One-Port Elements

As shown in [26], all commonly used linear one-port elements, including dynamic components such as capacitors and inductors, can be represented in the WD domain by means of their equivalent Thévenin model. Starting from the discrete-time Thévenin relation in the Kirchhoff domain

$$v[k] = R_{\mathrm{e}}[k]i[k] + V_{\mathrm{e}}[k]\,, \tag{6}$$

where k denotes the discrete-time index and $R_{\mathrm{e}}[k]$ and $V_{\mathrm{e}}[k]$ are the resistive and voltage parameters, respectively, and applying (1), the corresponding WD Thévenin representation can be derived as

$$b[k] = \frac{R_{\mathrm{e}}[k] - Z[k]}{R_{\mathrm{e}}[k] + Z[k]}a[k] + \frac{2Z[k]}{R_{\mathrm{e}}[k] + Z[k]}V_{\mathrm{e}}[k]\,. \tag{7}$$

The expressions of $R_{\mathrm{e}}[k]$ and $V_{\mathrm{e}}[k]$ depend on the specific element being modeled [26]. The instantaneous dependence between $b[k]$ and $a[k]$ in (7) can be removed by selecting $Z[k] = R_{\mathrm{e}}[k]$. Under this condition, (7) reduces to $b[k] = V_{\mathrm{e}}[k]$, and the element is said to be *adapted*.

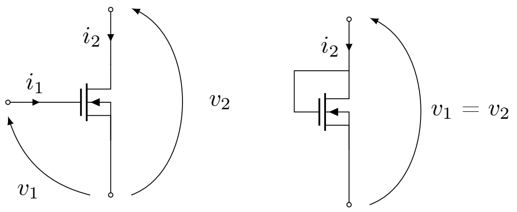
2.3. Modeling Nonlinear One-Port Elements: Diodes

Diodes are usually modeled by means of the *Extended Shockley model* [25], which, thanks to series and parallel resistors, R_{s} and R_{p}, reduces numerical errors encountered in the evaluation of exponential functions. The equation reads as follows

$$i = f(v, i) = I_{\mathrm{s}}\Big(\exp\Big(\frac{v - R_{\mathrm{s}}i}{\eta V_{\mathrm{t}}}\Big) - 1\Big) + \frac{v - R_{\mathrm{s}}i}{R_{\mathrm{p}}}\,, \tag{8}$$

where the sampling index k is omitted for the sake of clarity, I_{s} is the saturation current, η is the ideality factor, V_{t} is the thermal voltage. However, once (8) is turned into the WD domain, it cannot be adapted, and many different solutions have been presented in the literature to implement it in the WD domain, including Newton-Raphson solvers [25], Lambert $\mathcal{W}$ [31], and Wright ω functions [30]. In this work, instead, we employ Canonical Piecewise-Linear (CWPL) functions [23, 24].

Let us consider the diode $i - v$ characteristics we aim to represent in the WD domain, and let us select J significant points having coordinates $(v_{\mathrm{p}j}, i_{\mathrm{p}j})$, with $j = 1, \ldots, J$. We define $\mathbf{i}_{\mathrm{p}} = [i_{\mathrm{p}1}, \ldots, i_{\mathrm{p}J}]^{\mathrm{T}}$ as the vector of the current coordinates and $\mathbf{v}_{\mathrm{p}} = [v_{\mathrm{p}1}, \ldots, v_{\mathrm{p}J}]^{\mathrm{T}}$ as the vector of the voltage coordinates, both sorted in increasing order as we deal with monotonically increasing characteristics. We collect the slopes (i.e., resistance values) of the



(a) (b)

Figure 1: (a) Two-port model of an n-channel MOSFET; (b) one-port model of a diode-connected n-channel MOSFET.

different $J-1$ segments connecting the points in the vector $\mathbf{R}_{\text{p}} = [R_{\text{p}1}, \ldots, R_{\text{p}J-1}]^{\text{T}}$, where each parameter $R_{\text{p}j}$ is computed as

$$R_{\text{p}j} = \frac{\delta v_{\text{p}j}}{\delta i_{\text{p}j}}\,, \tag{9}$$

with $\delta v_{\text{p}j} = (v_{\text{p}j+1} - v_{\text{p}j})$ and $\delta i_{\text{p}j} = (i_{\text{p}j+1} - i_{\text{p}j})$. Starting from (1), the corresponding points in the WD domain are obtained as

$$\mathbf{a}_{\text{p}} = \mathbf{v}_{\text{p}} + Z_{\text{p}}\mathbf{i}_{\text{p}}\,, \quad \mathbf{b}_{\text{p}} = \mathbf{v}_{\text{p}} - Z_{\text{p}}\mathbf{i}_{\text{p}}\,, \tag{10}$$

where $\mathbf{a}_{\text{p}}$ and $\mathbf{b}_{\text{p}}$ are the vectors of incident and reflected waves, respectively, while Z_{p} is a free parameter properly chosen among the $R_{\text{p}j}$ values. If $Z_{\text{p}} > 0$, it can be verified that the points in the WD domain are still sorted in increasing order [24].

Having obtained the points in the WD domain, a CPWL representation of a generic scalar WD mapping $b = h(a)$ (without jump discontinuities) can be written as

$$b = \lambda_0 + \lambda_1 a + \sum_{j=1}^{J} \eta_j |a - a_{\text{p}j}|\,. \tag{11}$$

All the other parameters are defined as

$$\begin{aligned} &\lambda_1 = 0.5(m_0 + m_J)\,, \\ &\eta_j = 0.5(m_j - m_{j-1})\,, \qquad j = 1, \ldots, J\,, \\ &\lambda_0 = h(0) - \sum_{j=1}^{J} \eta_j |a_{\text{p}j}|\,, \end{aligned} \tag{12}$$

where m_j is the slope of the jth segment and it is computed as

$$m_j = \frac{b_{\text{p}j+1} - b_{\text{p}j}}{a_{\text{p}j+1} - a_{\text{p}j}}\,, \qquad j = 1, \ldots, J-1\,. \tag{13}$$

We also assume, without any loss of generality, that the slopes of the segments with index $j = 0$ and $j = J$, corresponding to the intervals $[-\infty, a_{\text{p}1}]$ and $[a_{\text{p}J}, +\infty]$, are $m_0 = m_1$ and $m_J = m_{J-1}$, respectively.

3. MODELING DIODE-CONNECTED MOSFETS

Fig. 1a shows a possible two-port model of an n-channel MOSFET, where v_1 and v_2 denote the gate-to-source and drain-to-source voltages, respectively, and i_1 and i_2 represent the gate and drain currents. An n-channel MOSFET operates in the conduction region when $v_1 > V_{\text{th}}$ holds true, with V_{th} being the threshold voltage required to form an inversion layer at the semiconductor-oxide interface [32].

Under this condition, the gate is insulated from the channel by the gate oxide, and its current can be neglected ($i_1 \approx 0$). The drain current i_2, on the other hand, depends on the drain-to-source voltage and obeys to the two following current-voltage relationships depending on the operating region [32]

$$\begin{cases} i_2 = k_{\text{n}}\left[(v_1 - V_{\text{th}})\,v_2 - \dfrac{v_2^2}{2}\right], & v_2 < v_1 - V_{\text{th}}\,, \\ i_2 = \dfrac{1}{2}k_{\text{n}}\,(v_1 - V_{\text{th}})^2\,(1 + \lambda v_2)\,, & v_2 \geq v_1 - V_{\text{th}}\,. \end{cases} \tag{14}$$

The first expression corresponds to the ohmic (linear) region, where the inversion channel extends along the entire length of the device, and the MOSFET behaves as a voltage-controlled resistor. The second expression, instead, describes the saturation region, in which the drain current i_2 is independent of v_2 until the channel pinch-off, where a mild linear dependence on v_2 is restored. Moreover, in (14) k_{n} denotes the transconductance parameter and λ is the coefficient representing the channel modulation.

Fig. 1b shows a diode-connected n-channel MOSFET, in which the gate and drain terminals are short-circuited so that $v_1 = v_2$. As a consequence, whenever the transistor is turned on, the condition $v_2 \geq v_1 - V_{\text{th}}$ is always satisfied, and the MOSFET necessarily operates in the saturation region. In this configuration, the device exhibits a nonlinear current-voltage characteristic similar to that of a diode, with a cubic dependence of the drain current on the applied voltage as

$$i_2 = \frac{1}{2}k_{\text{n}}\,(v_2 - V_{\text{th}})^2\,(1 + \lambda v_2)\,. \tag{15}$$

Compared to the exponential current-voltage relationship of a pn-junction diode, this cubic behavior results in a softer and more gradual increase in current. Such a characteristic is commonly exploited in audio circuits (e.g., in the Fulltone OCD pedal), where diode-connected MOSFETs are often used for clipping and overdrive stages as they produce a milder and more musically pleasing distortion.

Finally, it is worth pointing out that, since diode-connected MOSFETs are de facto one-port nonlinearities, they can be modeled by means of CPWL functions as explained in Sec. 2.3.

4. SOLUTION OF NONLINEAR WDFS

In general, the choice between an iterative or an explicit method depends on the number of nonlinear elements present in the WD structure. In particular, when a WDF contains multiple one-port nonlinearities, iterative techniques such as fixed-point [20, 33], Newton–Raphson [34, 35], or extended fixed-point [36] methods are typically employed to compute the solution at each operating point. Conversely, when the WDF contains a single one-port nonlinearity, the system can be solved without resorting to iterative solvers by exploiting the tree-like arrangement of the WD structure [22], with the nonlinear element placed at the root.

Such a choice is also related to the level of modularity one wants to achieve. Indeed, the same circuit can be represented in the WD domain using different numbers of nonlinear elements, depending on whether nonlinearities are grouped into a single block or treated individually [34, 13]. This modeling choice directly affects the structure of the WD representation and, consequently, the numerical method required to solve it. We here, thus, present two algorithms capable of addressing both scenarios.

4.1. Solving WDFs With Multiple One-Port Nonlinearities

Let us assume, without loss of generality, that the WDF contains a single topological junction with the nonlinear elements connected to its first P ports. The remaining ports, indexed from $P+1$ to N, are associated with linear elements, where N is the total number of circuit elements. Under this assumption, the corresponding connection tree [37] consists of a single *root*, which is the topological junction, and a set of *leaves* corresponding to both linear and nonlinear components. Before starting the iterative procedure, the port resistances of linear elements are initialized according to their adaptation conditions [38], while the port resistances associated with nonlinear elements are set to 1. In addition, we decide to initialize all wave variables and Kirchhoff variables to zero, namely $\mathbf{a}[0] = \mathbf{0}$, $\mathbf{b}[0] = \mathbf{0}$, and $\mathbf{v}[0] = \mathbf{0}$, where $\mathbf{v} = [v_1, \dots, v_N]^{\mathrm{T}}$ denotes the vector of port voltages. Then, the algorithm entails the following five stages at each discrete-time step k [20, 38]:

- *Initialization*: The waves reflected by linear elements are evaluated as $b[k] = V_{\mathrm{e}}[k]$ and remain fixed during the iterative process. The starting point of the iteration at the current sampling step is initialized using the wave and voltage values computed at $k-1$, namely
$$\mathbf{a}^{(0)}[k] = \mathbf{a}[k-1]\,, \qquad \mathbf{v}^{(0)}[k] = \mathbf{v}[k-1]\,. \tag{16}$$
- *Update of Z_p*: The port resistances of nonlinear elements Z_p are updated so as to approximate the local slope of the corresponding Kirchhoff i–v characteristic. In fact, in [25, 35] it is shown that such a choice significantly improves convergence speed in WDF simulations. This update is performed according to
$$Z_p[k] = v_p'(i_p[k-1])\,, \qquad p = 1, \dots, P\,, \tag{17}$$
where $v_p'(i_p[k-1])$ is the derivative of the voltage with respect to the current evaluated at the previous sampling step. As a final step, matrix $\mathbf{S}$ is recomputed since dependent on $\mathbf{Z}$.
- *Local Nonlinear Scattering Stage*: At each iteration, the reflected waves associated with nonlinear elements are computed according to their respective scattering relations as
$$b_p^{(\gamma)}[k] = f_p\left(a_p^{(\gamma-1)}[k]\right)\,, \qquad p = 1, \dots, P\,, \tag{18}$$
where $\gamma \geq 1$ denotes the iteration index and $f_p(\cdot)$ is the scattering function of the p-th nonlinear element. In this work, $f_p(\cdot)$ is the particular CPWL mapping employed to model the diode and the diode-connected MOSFETs.
- *Global Scattering Stage*: The waves incident to the elements are obtained by propagating the reflected waves via the scattering junction according to the selected iterative scheme. We can write the general global update rule as
$$\begin{aligned}\mathbf{a}^{(\gamma)}[k] =& \mathbf{a}^{(\gamma-1)}[k] + \\ & - \mathbf{K}(\mathbf{a}^{(\gamma-1)}[k])\,[\mathbf{a}^{(\gamma-1)}[k] - \mathbf{c}(\mathbf{a}^{(\gamma-1)}[k])]\,,\end{aligned} \tag{19}$$
where $\mathbf{c}(\mathbf{a}^{(\gamma-1)}[k]) = \mathbf{S}\mathbf{f}(\mathbf{a}^{(\gamma-1)}[k])$, $\mathbf{f}(\mathbf{a}) = [f_1(a_1), \dots, f_N(a_N)]^{\mathrm{T}}$ collects the waves reflected by all circuit elements, and $\mathbf{K}(\mathbf{a}^{(\gamma-1)}[k])$ is a matrix that is set according to the particular iterative method. In this work, we consider the Scattering Iterative Method (SIM) [25], i.e., a fixed-point method, for which we have $\mathbf{K}(\mathbf{a}^{(\gamma-1)}[k]) = \mathbf{I}$ [36].
- *Convergence Check*: Local Nonlinear Scattering and Global Scattering stages are iterated till the convergence condition
$$\left\| \mathbf{v}^{(\gamma)}[k] - \mathbf{v}^{(\gamma-1)}[k] \right\|_2 \leq \varepsilon_{\mathrm{SIM}} \tag{20}$$
is satisfied, with ε being a small tolerance (e.g., $\varepsilon_{\mathrm{SIM}} = 10^{-5}$ V).

4.2. Solving WDFs With a Single One-Port Nonlinearity

The main bottleneck of the algorithm presented in the previous subsection is the recomputation of the scattering matrix $\mathbf{S}$ performed at each time step k. Therefore, whenever possible, it is advantageous to group nonlinearities into a single nonlinear block and exploit a key property of WDFs: a WD structure containing at most one nonlinear element can be solved in a fully explicit fashion [22, 12, 13]. In this case, the WDF is still organized as a connection tree, but the nonlinear element acts as the *root*, the topological junction as the so-called *node*, and the linear one-port elements as the *leaves*.

Let us assume, without loss of generality, that the nonlinear element is connected to port 1 of the scattering junction, for which the implicit relations are removed by setting Z_1 such that $\mathbf{S}_{1,1} = 0$ holds true. The resulting algorithm closely resembles the one described in the previous subsection, and proceeds by traversing the connection tree from the leaves to the root and then backward. At the beginning, all wave variables are initialized to zero. Then, along the lines of what described in Sec.4.1, the following stages are performed at each time step k:

- *Initialization*: The waves incident to the elements are initialized as in Sec.4.1.
- *Leaves Scattering Stage*: The waves reflected by linear elements are computed as $b[k] = V_{\mathrm{e}}[k]$.
- *Forward Scattering Stage*: the wave incident to the root (i.e., the nonlinear block) and reflected by port 1 of the topological junction is computed as
$$a_1[k] = \mathbf{s}_1\mathbf{b}[k]\,, \tag{21}$$
where $\mathbf{s}_1$ is the first row of matrix $\mathbf{S}$, which is fixed and precomputed.
- *Root Scattering Stage*: The wave reflected by the root and incident to port 1 of the topological junction is computed as
$$b_1[k] = f_1(a_1[k])\,, \tag{22}$$
where $f_1(\cdot)$ is the explicit mapping selected to model the nonlinear block, e.g., a CPWL function.
- *Backward Scattering Stage*: The wave incident to the elements and reflected by the junction are computed as
$$\mathbf{a}[k] = \mathbf{S}\mathbf{b}[k]\,. \tag{23}$$

5. EMULATION OF THE FULLTONE OCD PEDAL

In this section, we present and compare two possible solutions for emulating the Fulltone OCD circuit. The first involves the iterative method presented in Sec. 4.1 to break the delay-free loops formed at the interconnections of nonlinear elements; the second leverages the possibility to model nonlinearities of the Fulltone OCD's clipping stage as a single one-port nonlinearity and to solve the resulting WDF using the method presented in Sec. 4.2.

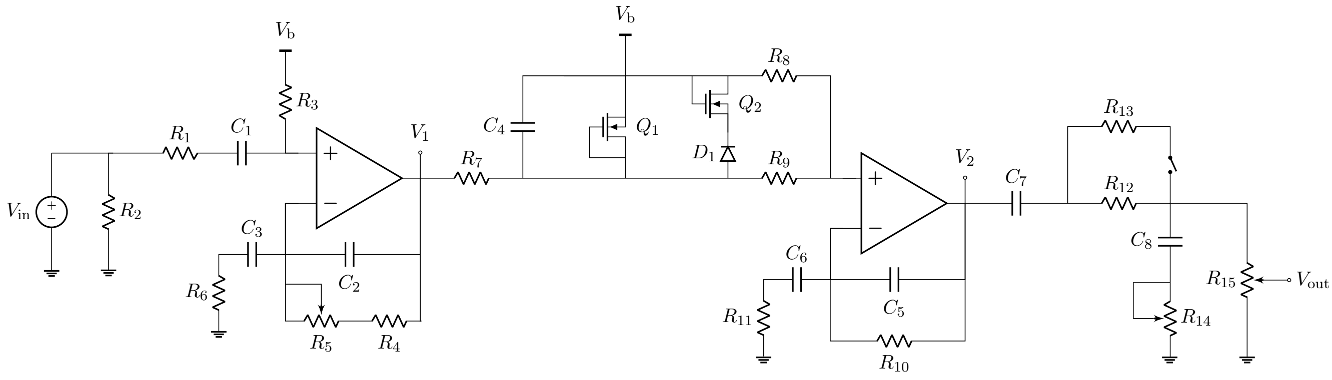


Figure 2: Circuit schematic of the Fulltone OCD pedal.

Table 1: Parameter values of the Fulltone OCD circuit shown in Fig. 2.

Param.	Value	Param.	Value	Param.	Value
R_1	10 kΩ	R_2	1 MΩ	R_3	470 kΩ
R_4	18 kΩ	R_5	500 kΩ	R_6	2.2 kΩ
R_7	10 kΩ	R_8	220 kΩ	R_9	10 kΩ
R_{10}	150 kΩ	R_{11}	39 kΩ	R_{12}	33 kΩ
R_{13}	22 kΩ	R_{14}	10 kΩ	R_{15}	500 kΩ
C_1	22 nF	C_2	220 pF	C_3	100 nF
C_4	10 nF	C_5	220 pF	C_6	100 nF
C_7	10 µF	C_8	47 nF	V_b	4.5 V

Table 2: Parameter values of diode 1N34A and MOSFET 2N7000.

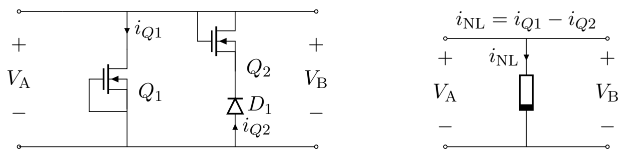
	Param.	Value	Param.	Value	Param.	Value
1N34A	I_s	2.58 µA	η	1.61	V_t	25.8 mV
	R_s	1 nΩ	R_p	1 TΩ	–	–
2N7000	k_n	0.025 A/V^2	V_{th}	2.1 V	λ	0.02

5.1. Fulltone OCD Circuit

Let us consider the Fulltone OCD (v2) schematic[1] shown in Fig.2, whose parameter values are reported in Table1. Owing to the presence of two operational amplifiers (opamps), the modeling and implementation of the circuit can be split, without a significant loss of accuracy, into three stages: (i) a linear input stage featuring the drive potentiometer R_5, characterized by the transfer function V_1/V_{in}; (ii) a nonlinear clipping stage comprising two diode-connected 2N7000 MOSFETs and a 1N34A germanium diode, whose parameters are listed in Table 2; and (iii) a linear output stage featuring the tone potentiometer R_{14} and the volume potentiometer R_{15}, characterized by the transfer function V_{out}/V_2.

Referring to Fig. 2, V_1 denotes the output voltage (node to ground) of the first stage and serves as the input to the second stage, while V_2 (node to ground) is the output of the second stage and the input to the third stage. In our experiments, the high-peak/low-peak switch in the output stage is assumed to be permanently closed.

[1]https://generalguitargadgets.com/pdf/ggg_ocdist_sc.pdf



(a) (b)

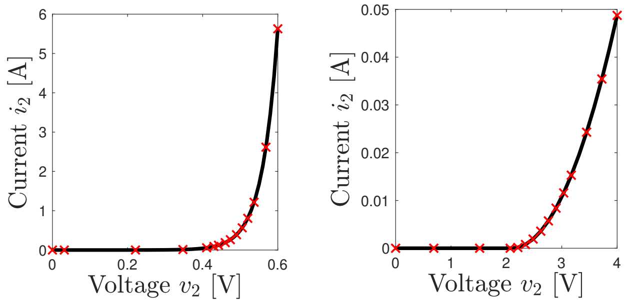
Figure 3: (a) Nonlinearities of the original Fulltone OCD's clipping stage; (b) single nonlinear element approximating the parallel connection in (a).

5.2. Modeling the Clipping Stage

The core of the clipping stage consists of a 2N7000 MOSFET connected in parallel with the series of a second 2N7000 MOSFET and a 1N34A germanium diode. Both MOSFETs are diode-connected, which allow us to model them as one-port elements in the WD domain.

Let us first consider the case in which we aim to model the stage respecting the modularity of the original circuit (case represented in Fig. 3a). To exploit the methodology presented in Sec. 2.3, we begin by selecting significant points on the device characteristic. We use an adaptive and non-uniform scheme that increases point density in regions of rapid slope variation. The sampling density is determined from a weighted combination of curve arc length and the magnitude of the second derivative. Then, points are selected to achieve the lowest mean absolute error for a given number of data. For the diode, we exploit (8) to extract 15 points, while, as far as MOSFETs are concerned, we exploit (15) to still extract 15 points, both represented with red crosses in Figs. 4(a) and 4(b), respectively.

Conversely, if we accept to give in the original circuit modularity, we can approximate the three nonlinear elements with a single one, passing from the subcircuit represented in Fig 3(a) to that of Fig 3(b). In order to obtain the characteristic of the new nonlinear element, we simulate the subcircuit in Fig 3(a) in Mathworks Simscape, and we apply the same methodology described above to extract 30 points. The nonlinear characteristic, together with the



(a) (b)

Figure 4: (a) Characteristic curve of diode 1N34A; (b) characteristic curve of a diode-connected MOSFET 2N7000. Red crosses mark the points selected to tune CPWL functions.

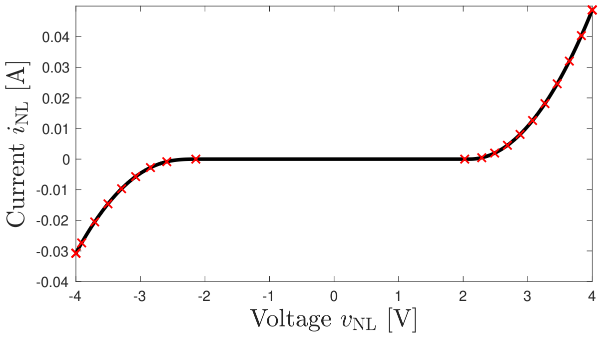


Figure 5: Characteristic curve of the equivalent nonlinear element represented in Fig. 3b consisting of the parallel connection between a diode-connected MOSFET 2N7000 and the series between a diode-connected MOSFET 2N7000 and a diode 1N34A (Fig. 3a). Red crosses mark the points selected to tune the CPWL function.

red crosses marking the selected points, is represented in Fig. 5. By looking at Figs. 4 and 5, we can appreciate the asymmetric clipping and the sharper characteristic of diode 1N34A with respect to the one of MOSFET 2N7000 when diode-connected. This is what granted the success to the guitar pedal since such a clipping stage provides a more complex, harmonic-rich, and slightly compressed tone, reminiscent of a cranked tube amplifier.

Finally, the extracted points are employed to tune the CPWL functions according to the approach presented in Sec. 2.3, yielding explicit nonlinear models that are later combined with the linear WDFs of the remaining circuit.

5.3. Results and Discussion

Although the proposed methodology was tested under different input amplitudes and frequencies, for illustrative purposes we here compare the performance of the WDFs solved using the iterative and explicit methods by considering a 1-second discrete-time sinusoid with amplitude 1 V, fundamental frequency 1 kHz, and sampling frequency $f_s = 96$ kHz as the input signal. Moreover, we select Backward Euler to discretize the time derivatives in dynamic elements, and we simulate the same circuit within

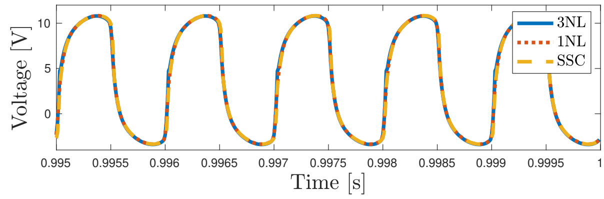


Figure 6: Last 5 ms of V_{out}: comparison between the output obtained with the implicit (3NL) and explicit (1NL) methods and within Simscape (SSC). The dashed yellow curve is overlapped to both the continuous blue (3NL) and dotted red (1NL) curves, confirming the accuracy of the WD implementations.

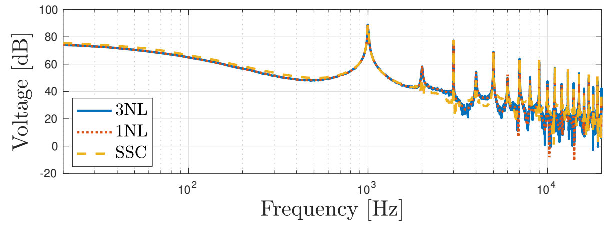


Figure 7: Discrete Fourier Transform (DFT) of V_{out} for 1 second of simulation. Curve convention is as in Fig. 6.

Mathworks Simscape using custom-made components to model the nonlinearities (Eqs. (8) and (15)).

Figs 6 and 7 show the output voltage V_{out} (only the last 5 ms) and its Discrete Fourier Transform (using the whole simulation), respectively, where the continuous blue curve represents the implicit method (3NL), the dotted red curve the explicit method (1NL), whereas the dashed yellow curve represents Simscape (SSC). The accuracy is not only confirmed by the good match between the curves but also by the Normalized Mean Squared Error of 3.0×10^{-3} (3NL) and 2.2×10^{-3} (1NL) as far as the time domain plot, and by the Log-Spectral Distance (LSD) [39] of 0.62 (3NL) and 0.56 (1NL) as for the frequency domain plot (over the range 20 Hz - 20 kHz). The slightly higher LSD observed for the explicit WDF can be attributed to the aggregation of nonlinearities into a single CPWL block, which introduces a marginal approximation in the frequency domain. Moreover, a visual inspection of Fig. 7 confirms that, for both methods, the harmonic components are correctly reproduced, with no missing or spurious peaks. Nonetheless, it is worth pointing out that such errors can be further reduced by increasing the number of breakpoints when tuning the CPWL functions, bearing in mind the trade-off between accuracy and computational cost. It is also worth to note that aliasing can be reduce by applying antiderivative antialiasing using the methodology proposed in [40].

As a second test, we run $R = 100$ identical runs for both the two methods (on an Apple Silicon M1 Pro processor), and we compute the average Real-Time Ratio (RTR),

$$\mathrm{RTR} = \frac{1}{R}\sum_{r=1}^{R}\frac{t_{\mathrm{sim},r}\, f_s}{K}\,, \tag{24}$$

where $t_{\mathrm{sim},r}$ is the simulation time of the r-th run, and K is the total number of samples. An RTR < 1 suggests that the algorithm can be run in real-time; conversely, RTR ≥ 1 suggests that real-time execution cannot be achieved. Once again, such a test is performed

Figure 8: Fulltone OCD plug-in on Ableton.

within the MATLAB environment. We obtain 3.12 and 0.14 for the implicit and explicit methods, respectively, pointing out the superior performance brought in by the latter methodology as it performs approximately 22x faster than the implicit method and 7x faster than real time (on the tested hardware).

The WDF implementation, developed as a plain MATLAB script, is available in our repository[2]. Audio examples, instead, can be found on a dedicated GitHub page[3]. Informal listening comparisons suggest no perceptually relevant differences between the output of the circuit simulated in Simscape (labeled "SSC") and that of our explicit WDF model (labeled "Ours") under the tested conditions. Finally, an audio plug-in (see Fig. 8) realized exploiting the JUCE framework is available on our repository, such that practitioners can take advantage of such a guitar pedal in their music productions.

6. CONCLUSIONS

In this article, we presented an explicit Wave Digital (WD) model of the Fulltone OCD pedal (v2). The proposed formulation exploits the possibility of grouping the nonlinear components of the asymmetric clipping stage into a single equivalent nonlinear element, thereby enabling an explicit realization of the corresponding WD structure. The resulting nonlinear characteristic was approximated by means of a Canonical Piecewise-Linear (CPWL) function, providing a compact explicit representation that can be evaluated without resorting to iterative solvers. To assess the benefits of the proposed modeling strategy, we compared two WD implementations: (i) a model preserving the three nonlinear one-port elements, requiring an iterative solution, and (ii) the proposed explicit model based on a single equivalent nonlinear element. Experimental validation against the reference Mathworks Simscape model showed that both approaches achieve high accuracy in the time and frequency domains, with low normalized mean squared error and close spectral agreement. At the same time, the explicit formulation substantially reduced the computational cost, achieving a significantly lower real-time ratio than the iterative implementation and demonstrating the great improvement of such a modeling strategy for real-time VA applications.

[2]`github.com/polimi-ispl/fulltoneocd`
[3]`polimi-ispl.github.io/fulltoneocd`

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