RESOLVING GROUPED NONLINEARITIES IN WAVE DIGITAL FILTERS USING ITERATIVE TECHNIQUES

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ABSTRACT

In this paper, iterative zero-finding techniques are proposed to resolve groups of nonlinearities occurring in Wave Digital Filters. Two variants of Newton's method are proposed and their suitability towards solving the grouped nonlinearities is analyzed. The feasibility of the approach with implications for WDFs containing multiple nonlinearities is demonstrated via case studies investigating the mathematical properties and numerical performance of reference circuits containing diodes and transistors; asymmetric and symmetric diode clippers and a common emitter amplifier.

1. INTRODUCTION

The Wave Digital Filter concept is a method for digitizing analog reference circuits. WDFs were originally developed in the 1970s with the intention of realizing digital lattice and ladder filter topologies [1] and, as such, were developed to preserve modularity and properties analogous to passivity and losslessness inherent in the analog prototype circuits being modeled [2]. Currently, WDFs are used extensively in virtual analog and physical modeling [3–11] for those same reasons. In 2015, a more general approach has been developed that deals with both multiple/multiport nonlinearities and arbitrary network topologies [12, 13].

The purpose of this paper is to build upon this general approach by incorporating an iterative solver into the WDF structure to solve the system of multiple/multiport nonlinearities. Newton's Method with backtracking is employed because it is a classic and robust zero-finding technique. Common models of the diode and transistor are studied to learn about the convergence properties using Newton's method of the underlying mathematical functions. Lastly, a case study of three simple reference circuits is presented which demonstrates the generality and promise for WDF implementation of circuits with multiple nonlinearities.

Section 2 summarizes the previous work related to WDFs with nonlinearities and reviews the general approach which the iterative method will be incorporated into. In Section 3, the setup of the iterative solver within the general approach is presented and the iterative techniques are introduced. Sections 4–5 present case studies of circuits containing a single diode, pair of diodes and a bipolar junction transistor. Section 6 summarizes the results.

2. PREVIOUS WORK

2.1. Nonlinear WDFs and Iterative Techniques

Many interesting musical devices contain nonlinear circuit elements and topologies which cannot be decomposed into only serial and parallel connections. Early approaches to developing WDF models with nonlinearities focused on reference circuits with certain types of single nonlinearities [14, 15]. Other solutions use domain knowledge about the device or circuit to make simplifying assumptions to realize computability of the WDF structure. These include combining multiple nonlinearities into a single one-port nonlinearity [5, 6, 9] and simplifying multiport nonlinearities into cross-control models [4, 7, 10]. A comprehensive overview of early nonlinear WDF implementations can be found in [15].

The first example of including a nonlinear circuit element in a WDF [14] involved attaching the nonlinearity to an adapted port at the root of the WDF. This is necessary because the model of the nonlinearity is delay free, and a port reflection back to the nonlinearity would create a delay-free loop. In addition, the nonlinearity studied was modeled with an invertible function in the Kirchhoff domain from which it was possible to map to a corresponding invertible function in the wave domain which was then able to be solved explicitly. In modern WDF structures, child elements in the WDF tree are adapted so that their upward-facing port is reflection free. The root element cannot be adapted so if the reference circuit contains a non-adaptable nonlinear or linear element it is placed at the root of a binary connection tree [4].

In [5], the Lambert $\mathcal{W}$ function is used to solve a single diode equation or approximate the solution to an anti-parallel diode equation. In particular, a lookup table is used to determine an initial guess at the solution which is then refined through iteration on an approximation of the Lambert $\mathcal{W}$ function. The case of multiple diodes is generalized and improved in [6].

In [3], a WDF implementation of a triode tube amplifier using the Cardarilli triode model is introduced. This method involves solving one or two nonlinear equations depending on whether or not grid current is taken into account. In both cases, the authors use the secant method to solve the nonlinear equations and, in the case where grid current is taken into account, multidimensional zero finding is avoided by solving one of the nonlinear equations first and using that result to determine whether or not the second nonlinear equation needs to be iterated on. This model was found to be more computationally efficient than previous attempts [7, 10] and perform more realistically, especially when in saturation.

Another approach to WDFs with multiple nonlinearities is provided in [16] where the passivity property of WDFs is exploited to show that WDFs are contractive systems which are guaranteed to converge to a fixed point under global iteration. Using this, they introduce an iteration time dimension and at each sample iterate along this dimension until the steady-state solution for that sample has been reached for each nonlinearity with all other circuit values held constant. While this approach can be applied to complex topologies that are expressible as non-tree-like arrangements of series and parallel adapters and models with multiple nonlinearities, the convergence of the fixed-point iteration is only linear

and the speed of convergence is highly dependent on the choice of port resistance. Additionally, the contractivity property only holds if the nonlinear elements are also contractive which excludes non-contractive nonlinearities such as transistors.

This approach is expanded upon in [17] where the unrelaxed fixed point iteration scheme is replaced with the secant method. They additionally modify the secant method to control the step in the search direction in a way such that it always moves in the direction of the zero. For multidimensional nonlinearities, two iteration schemes are proposed. In the first, the iteration of all nonlinearities is performed simultaneously in a vector formulation whereas in the second each nonlinearity is iterated on individually.

The first method was found to be faster when it did converge and the second method was found to converge in situations where the first method did not converge. The primary benefits of the methods in these two papers are that they preserve the modularity of the WDF structure whilst the second paper's results improves the convergence of the iterations from linear to superlinear.

Another iterative approach based on a graph theoretic analysis is given in [18]. In this approach, the entire circuit topology is represented with a single scattering parameter matrix and power waves are propagated between the circuit element ports. From this representation a fixed point iteration can then be performed to resolve the delay-free loops introduced by nonlinear elements.

An example of iterative techniques being used in the implementation of circuits containing single nonlinearities as state space filters is given in [19, 20]. This approach involves using the K-method to linearize the nonlinearities into a system of equations which can then be iterated on until convergence is reached with the desired unknown quantity. Newton's method is used to solve single antiparallel diode nonlinearities whereas pretabulated tables are suggested for realization of triodes and bipolar junction transistors (BJTs) in amplifier circuits.

2.2. A General Approach for Multiple/Multiport Nonlinearities with Arbitrary Topologies

We review a general approach to set up a WDF structure with any number of multiport nonlinearities as well as with any general topology [12, 13].

First, the prototype circuit must be analyzed and decomposed into parallel, series and rigidly connected components. This can be accomplished using graph theoretic techniques [12, 21]. For circuits containing multiple/multiport nonlinearities, all nonlinearities are rigidly connected using the replacement graph technique in [21] so that they are kept together as a single entity. The results of this process is an *SPQR* tree where all nonlinear elements are grouped together at the root of the tree in an $\mathcal{R}$-type node.

To deal with the nonlinearities in the $\mathcal{R}$-type node, all of the nonlinearities are pulled out of the $\mathcal{R}$-type node. This results in a system of vector nonlinearities attached to a $\mathcal{R}$-type adapter represented mathematically by the following system:

$$\text{wave nonlinearity} = \{\mathbf{a}_I = F_w(\mathbf{b}_I) \tag{1a}$$

$$\text{scattering} = \begin{cases} \mathbf{b}_I = \mathbf{S}_{11}\mathbf{a}_I + \mathbf{S}_{12}\mathbf{a}_E \\ \mathbf{b}_E = \mathbf{S}_{21}\mathbf{a}_I + \mathbf{S}_{22}\mathbf{a}_E \end{cases} \tag{1b}$$

$$\text{S matrix} = \begin{bmatrix} \mathbf{S}_{11} & \mathbf{S}_{12} \\ \mathbf{S}_{21} & \mathbf{S}_{22} \end{bmatrix}, \tag{1c}$$

where F_w represents the wave domain nonlinear equation(s), $\mathbf{a}_I$ and $\mathbf{b}_I$ represent the vectors of internal incident and reflected waves

and $\mathbf{a}_E$ and $\mathbf{b}_E$ represent the external incident and reflected waves. More specifically, all incident and reflected waves are defined in terms of the $\mathcal{R}$-type adapter with external waves propagating from the WDF subtree and internal waves from the nonlinearities.

As described in [13], to calculate the $\mathbf{S}$ matrix, it is first necessary to form an $\mathbf{X}$ matrix. This is done by attaching an instantaneous Thévenin port equivalent to each port of the $\mathcal{R}$-type adapter and then using Modified Nodal Analysis (MNA) to determine the contents of the $\mathbf{X}$ matrix. It follows from the definitions of waves and Thévenin port equivalents that $\mathbf{S}$ is given by the following matrix equation:

$$\mathbf{S} = \mathbf{I} + 2 \begin{bmatrix} \mathbf{0} & \mathbf{R} \end{bmatrix} \mathbf{X}^{-1} \begin{bmatrix} \mathbf{0} & \mathbf{I} \end{bmatrix}^T, \tag{2}$$

where $\mathbf{R}$ is a diagonal matrix of port resistances and $\mathbf{I}$ is the identity matrix.

Next, since most nonlinear circuit models are defined in the Kirchhoff domain and F_w may be hard to obtain, it may be easier to work with $\mathbf{i}_C = F_k(\mathbf{v}_C)$. In that case a w–K converter matrix $\mathbf{C}$ to convert incident and reflected waves $\mathbf{a}_I$ and $\mathbf{b}_I$ into voltage and currents $\mathbf{v}_C$ and $\mathbf{i}_C$ is typically used. The $\mathbf{C}$ matrix is given by:

$$\mathbf{C} = \begin{bmatrix} \mathbf{C}_{11} & \mathbf{C}_{12} \\ \mathbf{C}_{21} & \mathbf{C}_{22} \end{bmatrix} = \begin{bmatrix} -\mathbf{R}_I & \mathbf{I} \\ -2\mathbf{R}_I & \mathbf{I} \end{bmatrix}, \tag{3}$$

where $\mathbf{R}_I$ is a diagonal matrix of internal port resistances. This process results in three vector delay-free loops which can then be reduced to one vector delay-free loop by combining the submatrices of $\mathbf{S}$ and $\mathbf{C}$ into matrices $\mathbf{E}$, $\mathbf{F}$, $\mathbf{M}$ and $\mathbf{N}$:

$$\mathbf{E} = \mathbf{C}_{12}(\mathbf{I} + \mathbf{S}_{11}\mathbf{H}\mathbf{C}_{22})\mathbf{S}_{12} \tag{4a}$$

$$\mathbf{F} = \mathbf{C}_{12}\mathbf{S}_{11}\mathbf{H}\mathbf{C}_{21} + \mathbf{C}_{11} \tag{4b}$$

$$\mathbf{M} = \mathbf{S}_{21}\mathbf{H}\mathbf{C}_{22}\mathbf{S}_{12} + \mathbf{S}_{22} \tag{4c}$$

$$\mathbf{N} = \mathbf{S}_{21}\mathbf{H}\mathbf{C}_{21}, \tag{4d}$$

with $\mathbf{H} = (\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})^{-1}$.

This formulation yields a structure in which all nonlinearities in the circuit can be isolated together at the top of the WDF tree above the $\mathcal{R}$-type adapter. This leads to the following system with the nonlinearities represented in the Kirchhoff domain:

$$\begin{cases} \mathbf{i}_C = F_k(\mathbf{v}_C) & \text{(5a)} \\ \mathbf{v}_C = \mathbf{E}\mathbf{a}_E + \mathbf{F}\mathbf{i}_C & \text{(5b)} \\ \mathbf{b}_E = \mathbf{M}\mathbf{a}_E + \mathbf{N}\mathbf{i}_C, & \text{(5c)} \end{cases}$$

where $\mathbf{E}$, $\mathbf{F}$, $\mathbf{M}$ and $\mathbf{N}$ are given in (4). If trying to work directly from (5), dealing with the nonlinearity in the Kirchhoff domain, it must be determined how to evaluate the nonlinearity as it still contains a delay-free loop.

In [12], this delay-free loop is eliminated by means of the K-method. With the K-method, the nonlinearity is solved either using iteration or table lookup with pretabulated values of the nonlinear function.

The general approach proposed in [12, 13] allows any prototype analog circuit to be turned into a computable WDF structure regardless of topology or number of nonlinearities as long as the nonlinearities possess a functional model representation. Use of the K-method, however, implies a shear transformation of the nonlinearity models from the Kirchhoff domain to a domain consisting of pseudo-wave variable $\mathbf{p}$ and current $\mathbf{i}_C$. Thus, if solutions are tabulated in either domain, the table of solutions must be shear transformed to the other domain. Finding the correct value in the

sheared space can require complex search and interpolation methods. Additionally, the storage and computational requirements of multidimensional tables quickly becomes challenging as the number of dimensions increases.

3. ITERATIVE TECHNIQUES

3.1. The General Approach with Nonlinear Solver

An iterative solution to the nonlinearities contained in (5a) is presented as an alternative to storing tables and to introduce generality and the abilityto obtain solutions of a desired numerical precision. The zero-finding formulation of the system in Section 2.2 is obtained by substituting (5a) into (5b):

$$\mathbf{v}_C = \mathbf{E}\mathbf{a}_E + \mathbf{F}F_k(\mathbf{v}_C), \qquad (6)$$

and then solving the equation for zero to obtain:

$$H(\mathbf{v}_C) = \mathbf{E}\mathbf{a}_E + \mathbf{F}F_k(\mathbf{v}_C) - \mathbf{v}_C. \qquad (7)$$

This nonlinear function $H(\mathbf{v}_C)$ will give the values of $\mathbf{v}_C$ and $\mathbf{i}_C$ that solve the instantaneous relationship.

Consequently, using an iterative technique such as Newton's method to find the zero of (7) presents itself as a natural method for resolving the delay-free loop in the general framework presented in Section 2.2.

In using such a technique, having a good initial guess is crucial to the success of the zero-finding algorithm. In the context of (6) and (7), a typical choice would be:

$$\mathbf{v}_C^0(n) = \mathbf{E}\mathbf{a}_E(n-1) + \mathbf{F}F_k(\mathbf{v}_C(n-1)), \qquad (8)$$

where $\mathbf{v}_C^0(n)$ is the initial guess at the value of $\mathbf{v}_C(n)$. However, considering that $\mathbf{v}_C(n-1)$ has already been propagated down and back up the tree structure, the most current value of $\mathbf{a}_E$ is already known. Thus, another possible initial guess would be:

$$\mathbf{v}_C^0(n) = \mathbf{E}\mathbf{a}_E(n) + \mathbf{F}F_k(\mathbf{v}_C(n-1)). \qquad (9)$$

In the case studies in Sections 4 and 5 both initial guess choices will tested and investigated.

3.2. Newton's Method

The basis of Newton's method in a single dimension to find the zero x^* of a function f comes from the Taylor series expansion of f about x^* which leads to the recursive series of approximations of x^*:

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}, \qquad (10)$$

for which $x_n \to x^*$ as $n \to \infty$ given that f and the initial guess x_0 satisfy certain assumptions. The multivariate equivalent of Newton's method is:

$$\mathbf{X}^{k+1} = \mathbf{X}^k - J(\mathbf{X}^k)^{-1}F(\mathbf{X}^k), \qquad (11)$$

with $\mathbf{X} = (x_1, x_2, \ldots, x_n)^T$, $F = (f_1, f_2, \ldots, f_n)^T$ and where J is the Jacobian matrix of F and the superscript represents the current iterate.

In order for Newton's method to converge quadratically in the univariate case, it is necessary that f be twice continuously differentiable, that x^* is a simple zero of f (meaning that $f'(x^*) \neq 0$

and $f''(x^*) \neq 0$) and the initial guess x_0 is in a close enough neighborhood of the zero [22, p. 85].

The condition for having global convergence is given by f again being twice continuously differentiable as well as being an increasing, convex function that has a zero [22, p. 86]. For a function meeting these assumptions, the zero x^* is unique and can be reached with any initial guess.

In order to have superlinear convergence in the multivariate case, F must be continuously differentiable in a convex open set around a simple zero $\mathbf{X}^*$ as well as having a sufficiently close initial guess $\mathbf{X}^0$. Additionally, if F is Lipschitz continuously differentiable near $\mathbf{X}^*$ then, for sufficiently close $\mathbf{X}^0$, the convergence is quadratic [23, p. 276].

3.3. Newton's Method with Backtracking

Since the convergence of Newton's method depends on the proximity of the initial guess to a zero, attempts have been made to alter Newton's method to improve the convergence. One such algorithm is called Newton's method with backtracking or damped Newton's method.

The main idea behind the univariate version of this algorithm is to keep the linear approximation of the function from overshooting the zero. This is accomplished by performing a backtracking line search on the linear approximation of the function and ensuring that the norm of the function is being reduced at each iteration. Thus, rather than setting $x_{n+1} = x_n - f(x_n)/f'(x_n)$, the new iterate is set to $x_{n+1} = x_n - \alpha f(x_n)/f'(x_n)$ where $\alpha \in (0, 1]$. Starting with $\alpha = 1$, α is multiplied by 0.5 – or any value in $(0, 1)$ – until the following condition is met:

$$\left| f\left(x_n - \alpha f'(x_n)^{-1}f(x_n)\right) \right| \leq (1 - \alpha\mu)|f(x_n)|, \qquad (12)$$

where $\mu \in (0, 1)$. This condition is called the sufficient decrease condition and ensures that the next guess is moving closer to x^*.

In the multivariate case, the sufficient decrease criterion is given by

$$\left\| F\left(\mathbf{X}^K - \alpha^k J(\mathbf{X}^k)^{-1}F(\mathbf{X}^k)\right) \right\| \leq (1 - \alpha\mu)\|F(\mathbf{X}^k)\|. \qquad (13)$$

Newton's method with backtracking does achieve global convergence under certain assumptions about f [24]. Unfortunately, however, there are still a wide range of smooth functions for which global convergence is not guaranteed.

3.4. Improving the Initial Guess

As previously noted, Newton's method and Newton's method with backtracking depend on a good initial guess and being in a close neighborhood of the zero in order to achieve quadratic convergence.

In addition to the initial guess types discussed Section 3.1, an additional enhancement would be to use another more globally robust method to hone in on a better initial guess for Newton's method and then switch methods when the refined guess is sufficiently closer to the region of quadratic convergence. One way to accomplish this is by starting the iterations using a method called Steepest Descent.

The univariate Steepest Descent method [25, pp. 654–659] works by finding a value $\hat{x}$ that minimizes a merit function g. The merit function is chosen in such a way that $g(\hat{x}) = f(x^*) = 0$

Table 1: Diode Clipper Circuit Component Values

Circuit	Component		
	R_1	C_1	C_2
Clipper 1	$2.2\,\text{k}\Omega$	$0.01\,\mu\text{F}$	N/A
Clipper 2	$2.2\,\text{k}\Omega$	$0.01\,\mu\text{F}$	$0.47\,\mu\text{F}$

(a) Asymmetric Diode Clipper Schematic

(b) Symmetric Diode Clipper Schematic

(c) Asymmetric Diode Clipper WDF

(d) Symmetric Diode Clipper WDF

Figure 1: Diode Clipper Schematics and WDF Structures
(Dark Grey: Nonlinearities; Light Grey: $\mathcal{R}$-type Adapter)

and, thus, is also the solution to the original problem at hand. The following merit function is typically chosen:

$$g(x) = \frac{1}{2}f(x)^2 \,. \tag{14}$$

Successive approximations of $\hat{x}$ are found by moving in the direction of greatest decrease which is $-g'(x)$, the negative of the derivative of g. Backtracking is also employed so that the newest estimate of the minimizer does not overshoot and move away from the minimizer.

In the multivariate case, the merit function is given by

$$G(\mathbf{X}) = \frac{1}{2}F(\mathbf{X})^T F(\mathbf{X}) \,, \tag{15}$$

and the direction of greatest decrease is given by the negative gradient $-\nabla G(\mathbf{X})$.

This method used by itself will eventually converge to the minimum of the merit function (which corresponds to the zero of the original function, if it exists), but the convergence is only linear. Even given that, it still approaches the zero quickly enough that a few iterations can be enough to generate an initial guess for Newton's method which will quickly converge to the zero.

In the implementation of Steepest Descent used in this paper, a maximum number of iterations as well as a tolerance on the size of the norm of the merit function are given. Thus, the algorithm stops if the merit function has been sufficiently minimized or when the maximum number of iterations has been reached.

Other methods exist, such as the Secant method and Broyden's Method, which numerically approximate the derivative and Jacobian. Additionally, quasi-Newton methods exist which only evaluate the Jacobian once and then perform incremental numerical updates of it at each iteration. These methods can reduce the computational complexity of their corresponding algorithms but this may sometimes be at the expense of reduced convergence speed and/or loss of the roundoff error correction typically exhibited by Newton's method [25, ch. 10.3].

In the following case studies, the performance of methods from Sections 3.3 and 3.4 will be evaluated on a circuit containing a single diode, one containing antiparallel diodes and one containing a transistor. Additionally, the mathematical characteristics of the nonlinear models of the diode and transistor will be examined to determine whether any guarantees can be given to their convergence using the proposed iterative methods.

4. DIODE CLIPPER CIRCUITS

The wave-domain solution of the diode has been well-studied in literature [4–6, 8, 9, 12, 16, 17, 26–28] and an explicit solution exists using the Lambert $\mathcal{W}$ function [5, 6] (although the Lambert $\mathcal{W}$ function requires an iterative method to either precalculate for table lookup or solve at runtime). While the solution to the diode can be tabulated in the wave domain, as has been previously done, it will be informative to demonstrate the method of Section 3.1 on
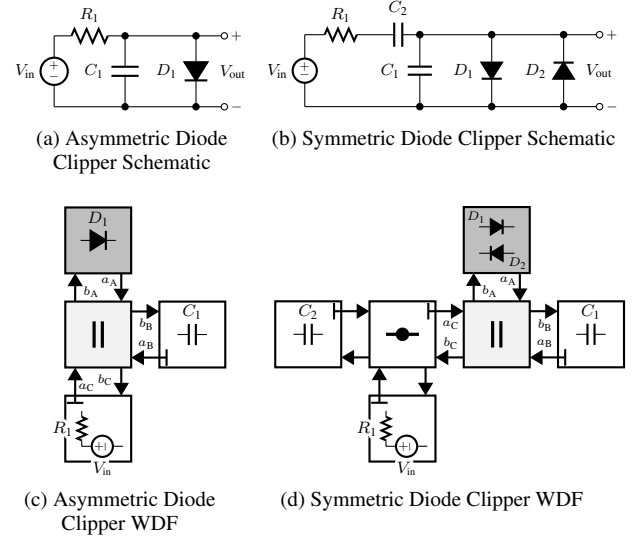
a circuit containing a single nonlinearity. Additionally, the mathematical properties of Shockley's diode model can be investigated.

An asymmetric diode clipper circuit consists of a resistive voltage source in parallel with a capacitor and a diode (Fig. 1a). We model the diode using the Shockley diode equation:

$$i_D = I_s\left(e^{v_D/\eta V_T} - 1\right) \,, \tag{16}$$

where $I_s = 2.52 \times 10^{-14}$ represents the reverse bias saturation current, $V_T = 0.02585$ represents the thermal voltage, η is the ideality factor of the diode and v_D is the voltage across the diode.

The scattering behavior of a parallel three-port adapter, which is already known in explicit form [29], immediately gives us the S matrix from the formulation of Section 2.2:

$$\mathbf{S} = \left[\begin{array}{c|c} \mathbf{S}_{11} & \mathbf{S}_{12} \\ \hline \mathbf{S}_{21} & \mathbf{S}_{22} \end{array}\right] = \left[\begin{array}{c|cc} \delta_A - 1 & \delta_B & \delta_C \\ \hline \delta_A & \delta_B - 1 & \delta_C \\ \delta_A & \delta_B & \delta_C - 1 \end{array}\right] \,. \tag{17}$$

where

$$\delta_m = \frac{2G_m}{G_A + G_B + G_C} \,. \tag{18}$$

From (3) it follows that the $\mathbf{C}$ matrix is:

$$\mathbf{C} = \begin{bmatrix} -R_A & 1 \\ -2R_A & 1 \end{bmatrix} \,. \tag{19}$$

The WDF (Fig. 1c) is formed by placing the diode at the unadapted port of the parallel adapter and then forming the system from (5).

From (7), the following equation representing the nonlinearity is determined:

$$\begin{aligned} h(\mathbf{v}_C(n)) &= \mathbf{E}\mathbf{a}_E(n) + \mathbf{F}f_k(\mathbf{v}_C(n)) - \mathbf{v}_C(n) \\ &= \mathbf{E}\mathbf{a}_E(n) + \mathbf{F}\left[I_s\left(e^{\mathbf{v}_C(n)/\eta V_T} - 1\right)\right] - \mathbf{v}_C(n) \,. \end{aligned} \tag{20}$$

From (20) it follows that

$$h'(\mathbf{v}_C(n)) = \mathbf{F}\frac{I_s}{\eta V_T}e^{\mathbf{v}_C(n)/\eta V_T} - 1 \,, \tag{21}$$

$$h''(\mathbf{v}_C(n)) = \mathbf{F}\frac{I_s}{(\eta V_T)^2}e^{\mathbf{v}_C(n)/\eta V_T} \,, \tag{22}$$

Table 2: Newton's Method with Backtracking Diode Clipper

Circuit	Upsamp	Iterations		Backtracking		Output Error	
		Mean	Peak	Mean	Peak	RMSE	Peak
Clipper 1	$1 \times f_s$	3.88	9	1.50	13	0.40	0.88
Clipper 1	$2 \times f_s$	3.01	9	0.57	9	0.14	0.47
Clipper 1	$4 \times f_s$	2.61	8	0.22	6	0.05	0.25
Clipper 1	$8 \times f_s$	2.32	7	0.07	5	0.02	0.05
Clipper 2	$1 \times f_s$	5.63	9	1.46	7	0.21	0.60
Clipper 2	$2 \times f_s$	4.61	7	0.74	5	0.08	0.26
Clipper 2	$4 \times f_s$	3.97	7	0.27	5	0.01	0.04
Clipper 2	$8 \times f_s$	3.23	6	0.08	2	0.01	0.04

Input signal: 10 kHz, 4.5 peak amplitude sinusoid at 44.1 kHz sampling rate,

are the equations for the first and second derivatives, respectively. Since I_S, $(\eta V_T)^2$ and $e^{\mathbf{v}_C(n)/\eta V_T}$ are all positive, it is clear that as long as $\mathbf{F} \neq \begin{bmatrix} 0 \end{bmatrix}$, then the diode model is either strictly convex or strictly concave. In either case, from the results in Section 3.2 it follows that (20) is globally convergent if that condition holds for the $\mathbf{F}$ matrix. In particular, the only way for $\mathbf{F} = \begin{bmatrix} 0 \end{bmatrix}$ is if $\mathbf{S}_{11} = \begin{bmatrix} -1 \end{bmatrix}$ which should never happen in practice. In the case of a parallel adapter, that condition would only be possible if G_A, the inverse of the port resistance R_A, of the diode's port, is equal to zero. The requirement that $R_A > 0$ prevents that from happening. In any arbitrary circuit topology, one should be able to explicitly set G_A to avoid the degenerate condition $\mathbf{F} = \begin{bmatrix} 0 \end{bmatrix}$.

A symmetric diode clipper circuit (Figs. 1b, 1d) contains two antiparallel diodes which (if identical) can be represented with the following model:

$$i_D = I_S \left(e^{v_D/\eta V_T} - e^{-v_D/\eta V_T} \right) . \qquad (23)$$

While the derivative is nonnegative:

$$\frac{\mathrm{d}}{\mathrm{d}v_D} i_D = \frac{I_S}{\eta V_T} \left(e^{v_D/\eta V_T} + e^{-v_D/\eta V_T} \right) > 0 \qquad (24)$$

$$\iff e^{v_D/\eta V_T} > -e^{-v_D/\eta V_T} , \qquad (25)$$

from the equation for the second derivative:

$$\frac{\mathrm{d}^2}{\mathrm{d}v_D^2} i_D = \frac{I_S}{(\eta V_T)^2} \left(e^{v_D/\eta V_T} - e^{-v_D/\eta V_T} \right) , \qquad (26)$$

it is easy to see that the second derivative takes on all values in $\mathbb{R}$ and so the function is not convex.

In the general setting of a circuit containing M_{fwd} parallel diodes and M_{rev} antiparallel diodes [6], the function for the nonlinearity is:

$$i_D = I_S[e^{v_D/M_{\mathrm{fwd}}\eta V_T} - e^{-v_D/M_{\mathrm{rev}}\eta V_T}] , \qquad (27)$$

from which the same conclusions can be reached. Therefore, global convergence is not guaranteed for any combination of parallel and antiparallel diodes.

Numerical simulations were run for WDF implementations of both diode clipper circuits. The numerical values used in the simulations are given in Table 1 where Clipper 1 refers to the asymmetric diode clipper and Clipper 2 refers to the symmetric diode clipper. The device values and ideality factor of 1.75 are the same as were used in [9].

For both diode clipper circuits, an LTspice [30] simulation was ran for use as a baseline comparison to the WDF simulations. The
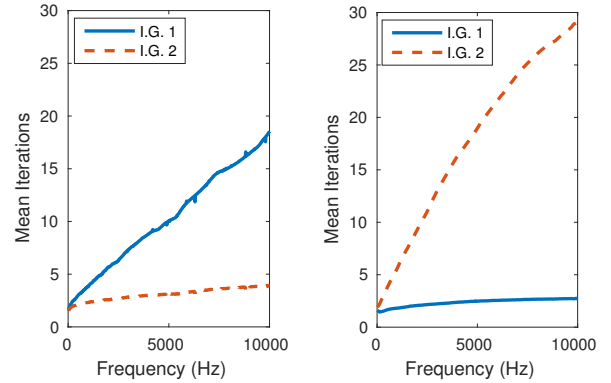
(a) Asymmetric Diode Clipper (b) Common Emitter Amplifier

Figure 2: Initial Guess Type Performance Comparison
(I.G. 1 refers to (9) and I.G. 2 refers to (8))

input voltage was a 10 kHz sinusoid with peak amplitude of 4.5 V which was used to test the performance of the iterative technique in response to a numerically challenging input signal. The LTspice simulations were generated using default LTspice configuration values with a maximum timestep frequency 176.4 kHz which reduces the interpolation error resulting from converting the adaptive timestep of the LTspice output to a fixed timestep.

Both Newton's method with backtracking and the hybrid Steepest Descent–Newton's method with backtracking algorithms were compared. For both algorithms, the tolerance (which is calculated as the L^2 norm of (7)) was set to 1.42×10^{-8} V [1] and maximum Newton iterations and backtracking steps were set to 200 and 50, respectively.

The results of the simulations for Newton's Method with backtracking are given in Table 2 where the error value is calculated as the difference in output voltage between the LTspice simulation and the WDF. RMSE is the root-mean-square error which is given by

$$E_{\mathrm{RMSE}} = \sqrt{\frac{\sum_{n=0}^{N-1}(x_{\mathrm{LT}}(n) - x_{\mathrm{WDF}}(n))^2}{N}} , \qquad (28)$$

where x_{LT} is the LTspice output voltage signal and x_{WDF} is the WDF output voltage. The peak error is calculated as the L^∞ norm of the difference in output voltages and is given by

$$E_{\mathrm{PEAK}} = \max_n |x_{\mathrm{LT}}(n) - x_{\mathrm{WDF}}(n)| . \qquad (29)$$

In both error formulas (28) and (29), x_{LT} refers to the LTspice output voltage, x_{WDF} refers to the WDF output voltage and N is the length of the signal in samples.

Even with this relatively high voltage and high frequency test signal, acceptable iteration counts are achieved after 4 to 8 times oversampling. The error values are the result of a combination of factors including linear interpolation and the fact that WDFs use the bilinear transform while LTspice does not. Results with lower amplitude and lower frequency test signals yielded extremely fast convergence with mean iterations typically between 1 or 2.

The results of the hybrid Steepest Descent–Newton's method (using the same 10 kHz sinusoid input signal) are given in Table 4.

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[1]approximately the square root of machine epsilon in Matlab R2015b

Table 3: Newton's Method Common Emitter Amp Simulation Results

Freq.	Amp.	Iterations		Backtracking		Error	
		Avg	Peak	Avg	Peak	Avg	Peak
10 Hz	0.01V	1.00	2	0.00	0	0.0001	0.0004
10 Hz	0.1V	1.14	2	0.00	0	0.0015	0.0045
10 Hz	1V	1.69	2	0.00	0	0.0168	0.0630
100 Hz	0.01V	1.90	2	0.00	0	0.0025	0.0039
100 Hz	0.1V	1.98	2	0.00	0	0.0273	0.0588
100 Hz	1V	1.59	11	0.01	5	0.0835	1.1007
1 kHz	0.01V	2.00	2	0.00	0	0.0086	0.0137
1 kHz	0.1V	2.56	3	0.00	0	0.0889	0.4006
1 kHz	1V	2.31	30	0.45	105	0.1063	1.6206
10 kHz	0.01V	2.87	3	0.00	0	0.0093	0.0169
10 kHz	0.1V	3.48	5	0.00	0	0.1609	0.6769
10 kHz	1V	N/A	N/A	N/A	N/A	N/A	N/A

The number of maximum Steepest Descent algorithm iterations were set to 2, 4 and 8 to illustrate the impact that Steepest Descent has on reducing the mean number Newton iterations. The amount of backtracking required by the Steepest Descent portion of the algorithm did appear to increase somewhat rapidly with the increase in maximum allowable iterations. There are, however, a number of ways to perform the backtracking line search portion of the algorithm so it may be possible to reduce the amount of backtracking by implementing one of those different methods.

Overall, the hybrid algorithm achieves a significant reduction in the number of Newton's method iterations required, particularly when combined with oversampling and a modest amount of Steepest Descent iterations.

Regarding choice of initial guess, Fig. 2a shows that Newton's method required fewer iterations for the asymmetric diode clipper when using the incident wave value from the previous timestep in the initial(8). This result was observed over a wide range of frequencies for tests being run using half-second long sinusoidal signals with peak amplitude of 4.5 V and was also seen when the same tests were ran on the symmetric diode clipper WDF.

5. MULTIPORT NONLINEARITIES–BIPOLAR JUNCTION TRANSISTOR

In this section, a common emitter amplifier is simulated using the method developed in Section 3.1. The circuit contains an NPN BJT which has base, collector and emitter terminals (Fig. 3a) and can be viewed as a two-port network device with ports BC and BE (Fig. 3b). The BJT's behavior is completely described by the voltages across the two terminals: v_{BE} and v_{BC}, which are the voltage from base to emitter and base to collector, respectively. The nonlinear behavior of the BJT was simulated using the Ebers–Moll model:

$$i_E = -I_s[e^{v_{BC}/V_T} - 1] + \frac{I_s}{\alpha_F}[e^{v_{BE}/V_T} - 1] \qquad (30a)$$

$$i_C = -\frac{I_s}{\alpha_R}[e^{v_{BC}/V_T} - 1] + I_s[e^{v_{BE}/V_T} - 1] \qquad (30b)$$

$$i_B = \frac{I_s}{\beta_R}[e^{v_{BC}/V_T} - 1] + \frac{I_s}{\beta_F}[e^{v_{BE}/V_T} - 1] , \qquad (30c)$$

where

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \text{ and } \beta_R = \frac{\alpha_R}{1 - \alpha_R} . \qquad (31)$$

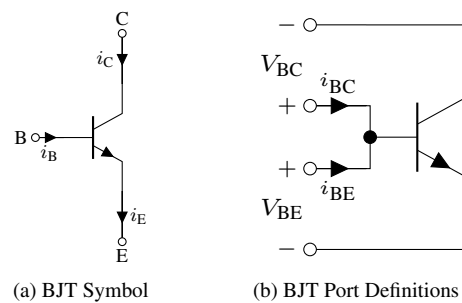(a) BJT Symbol   (b) BJT Port Definitions

Figure 3: Circuit element and network two-port of BJT

Since any one of the three equations in (30) can be derived from the other two, only two of them are needed to completely characterize the system. The values i_C and i_E are chosen in order to determine the current at the collector and emitter in terms of the current at the base.

The polarity of the currents given by the Ebers–Moll model (Fig. 3a) are not identical to the polarities of port currents when viewing the transistor as a two-port device (Fig. 3b). Port currents i_{textBC} and i_{BE} are found from the terminal currents i_C and i_E by

$$i_{BC} = -i_C \quad \text{and} \quad i_{BE} = i_E .$$

Following the method of Section 2.2, the reference circuit (Fig. 4a) was decomposed by isolating the two ports of the transistor above an $\mathcal{R}$-type adapter with series and parallel connections of linear components hanging below it (Fig. 4b).

Once the scattering behavior of the $\mathcal{R}$-type adapter was determined, the nonlinear equations were set up in the form of (7) leading to a complete WDF system; albeit one containing an implicit multidimensional delay-free loop.

The zero-finding equation F_k for (7) is:

$$F_k(\mathbf{v}_C) = \begin{bmatrix} \frac{I_s}{\alpha_R}\left(e^{v_{BC}/V_T} - 1\right) - I_s\left(e^{v_{BE}/V_T} - 1\right) \\ -I_s\left(e^{v_{BC}/V_T} - 1\right) + \frac{I_s}{\alpha_F}\left(e^{v_{BE}/V_T} - 1\right) \end{bmatrix} , \qquad (32)$$

and $\mathbf{v}_C = (v_{BC}, v_{BE})^T$.

The device parameters used for the simulations are given in Table 5 and component values for a 2N2222 transistor were used in the BJT model. Those values are $I_s = 1.0 \times 10^{-14}$, $\beta_F = 200$ and $\beta_R = 3$. The WDF digitization of the common emitter amplifier was analyzed by running a variety of sinusoidal input signals at different frequencies and peak amplitudes at a sampling rate of 44.1 kHz. The results are given in Table 3. Figure 2b shows that using the initial guess given by (9) results in fewer iterations with this circuit for an input sinusoid with peak amplitude of 0.5 V at a variety of frequencies. This is contrast to the result for both diode clipper circuits in which (8) performed better.

Newton's method with backtracking performed very well at frequencies up to 1 kHz with peak amplitudes up to 1 V. The method began to break down at higher frequency and amplitude combinations due to the procedure producing numbers which were unable to be represented by Matlab's double precision data type. Thus, the breakdown was not in Newton's method being unable to converge based on the provided initial guess but in a limitation of the numerics of the system being used for simulation. Using
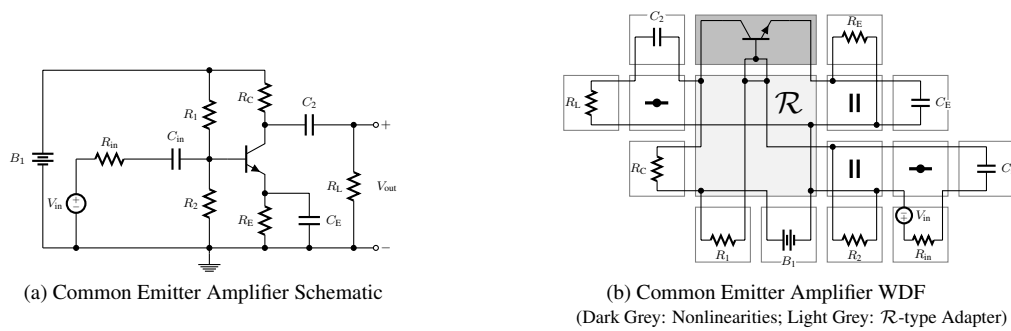
(a) Common Emitter Amplifier Schematic

(b) Common Emitter Amplifier WDF
(Dark Grey: Nonlinearities; Light Grey: $\mathcal{R}$-type Adapter)

Figure 4: Common Emitter Amplifier Schematic and WDF Structure

Table 4: Hybrid Steepest Descent–Newton's Method Diode Clipper Iteration Results

| | | Steepest Descent | | | | Newton's Method | | | |
| | | Iterations | | Backtracking | | Iterations | | Backtracking | |
Circuit	Oversampling	Max	Mean	Mean	Peak	Mean	Peak	Mean	Peak
Clipper 1	$1 \times f_s$	2	2.00	2.39	25	2.61	9	1.42	13
Clipper 1	$1 \times f_s$	4	3.07	22.54	89	1.55	8	0.77	11
Clipper 1	$1 \times f_s$	8	3.99	43.65	135	0.35	5	0.00	0
Clipper 1	$8 \times f_s$	2	2.00	7.45	31	1.20	6	0.03	3
Clipper 1	$8 \times f_s$	4	2.60	36.32	95	0.18	3	0.00	0
Clipper 1	$8 \times f_s$	8	2.63	42.09	107	0.00	1	0.00	0
Clipper 2	$1 \times f_s$	2	2.00	5.37	25	3.79	7	0.76	4
Clipper 2	$1 \times f_s$	4	3.73	36.60	91	1.50	5	0.01	1
Clipper 2	$1 \times f_s$	8	4.44	78.80	121	0.01	1	0.00	0
Clipper 2	$8 \times f_s$	2	2.00	11.05	29	2.01	5	0.01	1
Clipper 2	$8 \times f_s$	4	2.92	57.84	81	0.15	2	0.00	0
Clipper 2	$8 \times f_s$	8	2.94	61.60	99	0.03	1	0.00	0

Table 5: Common Emitter Amp Component Values

Component	Value
B_1	$18\,\mathrm{V}$
R_{in}	$1\,\mathrm{k\Omega}$
C_{in}	$50\,\mathrm{\mu F}$
R_1	$27.35\,\mathrm{k\Omega}$
R_2	$2.65\,\mathrm{k\Omega}$
R_E	$220\,\Omega$
C_E	$100\,\mathrm{\mu F}$
R_C	$1.78\,\mathrm{k\Omega}$
C_2	$10\,\mathrm{\mu F}$
R_L	$1\,\mathrm{k\Omega}$

Steepest Descent to improve the initial guess provided to Newton's method had no affect on the numerical limitation.

It should also be noted that the common emitter amplifier is designed to purely amplify small amplitude signals and is not designed to clip them. Since asymmetry can be seen in the peaks of a sinusoidal signal with amplitude of 0.2 V, it should be noted that a 1 V peak amplitude test signal would probably not be used in this circuit in practice and was used as a means of investigating the limits of the performance of Newton's method on a WDF containing an Ebers–Moll transistor model. A time domain output comparison of LTspice and the WDF simulation is given in Figure 5.

6. CONCLUSION

In this paper an iterative zero-finding technique was incorporated into a generalized WDF approach to digitizing analog reference circuits of arbitrary topology containing multiple/multiport nonlinearities. We elaborated on the work in [12, 13] by introducing two variations of Newton's method that show promise towards the realization of real-time WDFs with multiple nonlinearities. Newton's Method with backtracking was employed in addition to a variant where the Steepest Descent algorithm obtains better initial guesses and increases the speed of convergence.

Two different types of initial guesses were proposed for which (8) resulted in fewer iterations in both the asymmetric and symmetric diode clipper WDFS and (9) resulted in fewer iterations for the common emitter amplifier WDF. For the circuit simulated in [11], tests also indicated fewer iterations using (9) [2]. Both initial guess

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[2]Private Communication with W. Ross Dunkel, Jun. 10, 2016
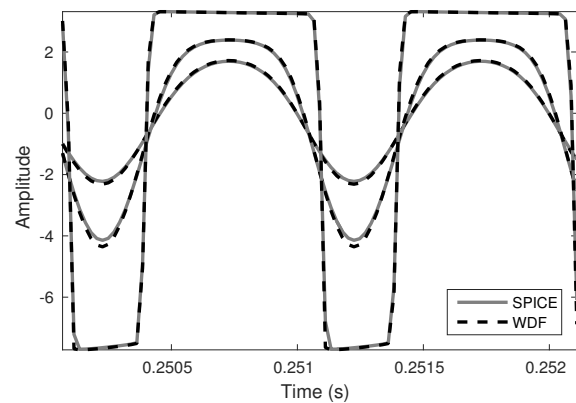
Common Emitter Amplifier Output

Figure 5: Two cycles of output voltage from 1 kHz input sinusoid

types should be tested to determine which one performs better for a particular WDF implementation.

We were able to show that the Shockley diode equation meets the requirements for global convergence with Newton's Method and that both algorithms employed in this paper yielded rapid convergence in an asymmetric diode clipper test circuit. Numerical results additionally indicated that a pair of identical antiparallel diodes treated as a singular nonlinearity exhibited good convergence characteristics even when tested with high frequency and amplitude test signals in a symmetric diode clipping circuit.

Additionally, the numerical performance of the Ebers–Moll model of a BJT was studied via implementation of a common emitter amplifier circuit. Newton's Method with backtracking performs efficiently for signals that fall within and slightly outside the standard operating range of the amplifier circuit.

While the recent work of Schwerdtfeger and Kummert [17] preserves the modularity of the WDF structure, the convergence rate of the methods can be sensitive to the values chosen for the port resistances of the nonlinear elements.

The choice of port resistances for nonlinearities in the proposed approach does not exhibit that same sensitivity. Since the delay-free loop being resolved is restricted to the system of nonlinearities and isolated from the rest of the WDF, impedance mismatching does not occur in the presented approach. The only restriction on the nonlinear port resistances is that they must be chosen such the **F** matrix does not get set to zero. There is no inherent restriction on the number of nonlinearities that can be included.

While this paper focused on developing the theory and simple examples illustrating the proposed technique, higher dimensional nonlinearities have already been successfully tested. These include the first clipping stage of the Big Muff Pi distortion pedal [12] and the preamp of the Fender Bassman amplifier [11]. A real-time WDF software library using the presented approach has also been recently developed [31].

The only caveats of the presented method for handling nonlinearities in WDFs are that the properties of the multivariate nonlinear systems must allow them to be solved with iterative techniques and that the iterative techniques are computationally tractable.

7. ACKNOWLEDGMENTS

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